National Semiconductor

June 3, 2008

LM48556 Boomer® Audio Power Amplifier Series
Fully Differential, Mono, Ceramic Speaker Driver

General Description

The LM48556 is a single supply, mono, ceramic speaker driver with an integrated charge-pump, designed for portable devices, such as cell phones, where board space is at a premium. The LM48556 charge pump allows the device to deliver 17.5V_{PP} (typ) from a single 4.5V supply. Additionally, the charge pump features a soft start function that minimizes transient current during power-up.

The LM48556 features high power supply rejection ratio (PSRR) of 80dB at 217Hz, allowing the device to operate in noisy environments without additional power supply conditioning. Flexible power supply requirements allow operation from 2.7V to 4.5V. Additionally, the LM48556 features a differential input function and an externally configurable gain. A low power shutdown mode reduces supply current consumption to 0.1µA.

Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48556 is available in an ultra-small 12-bump micro SMD package (2mm x 1.5mm).

Key Specifications

- Output Voltage Swing
  - V_{DD} = 3.6V, 1kHz — 14.2V_{PP} (typ)
  - V_{DD} = 4.5V, 1kHz — 17.5V_{PP} (typ)
- Power Supply Rejection Ratio f = 217Hz, V_{DD} = 3.6V — 80dB (typ)
- I_{DD} at V_{DD} = 3.6V — 4.8mA (typ)
- Wake-Up Time — 0.5ms (typ)

Features

- Fully differential amplifier
- Externally configurable gain
- Integrated charge pump
- Low power shutdown mode
- Soft start function

Applications

- Mobile phones
- PDA's
- Digital cameras

Typical Application

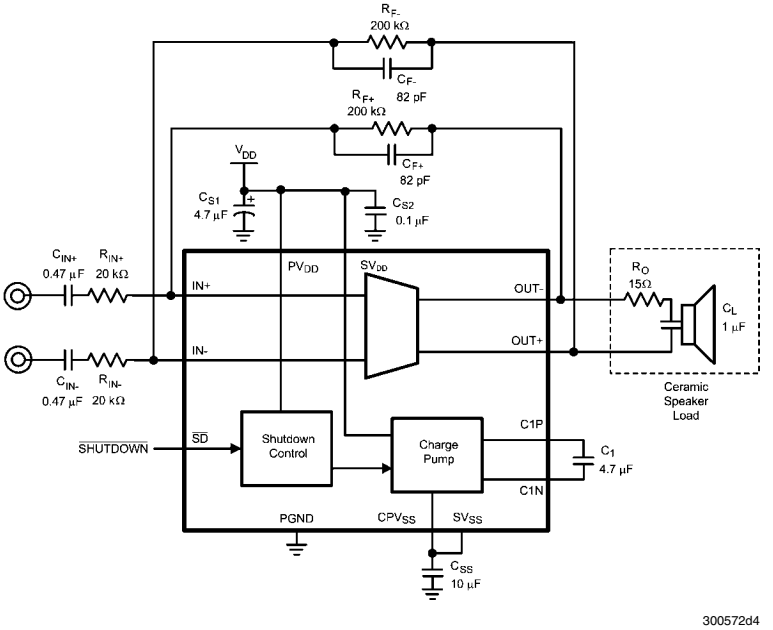

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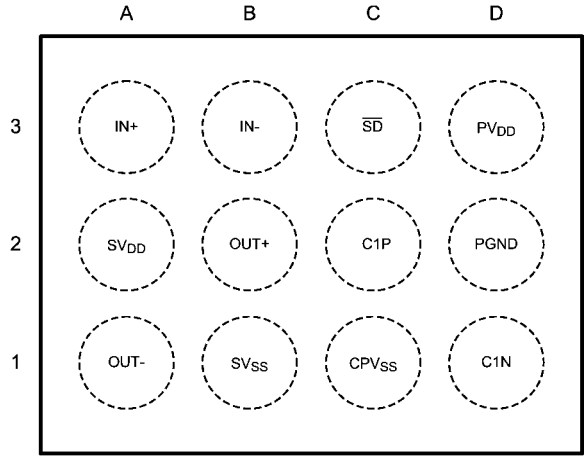
FIGURE 1. Typical Audio Amplifier Application Circuit

Boomer® is a registered trademark of National Semiconductor Corporation.

Connection Diagrams

12 Bump micro SMD



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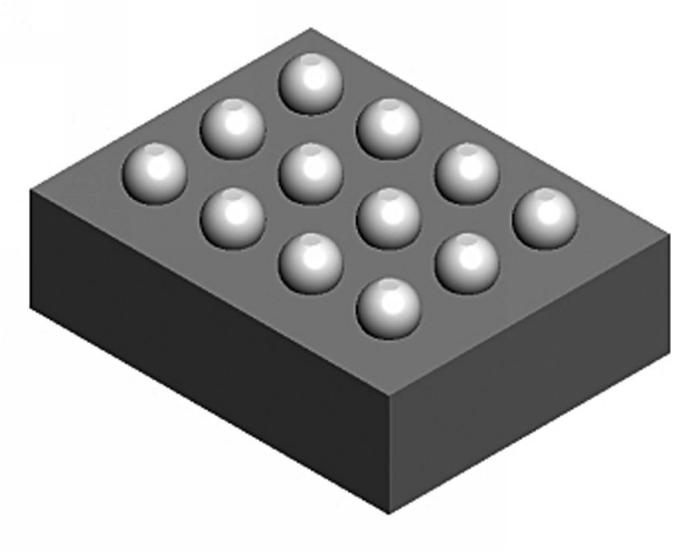
Top View
Order Number LM48556TL, LM48556TLX
See NS Package Number TLA121AA

12 Bump micro SMD
Package View



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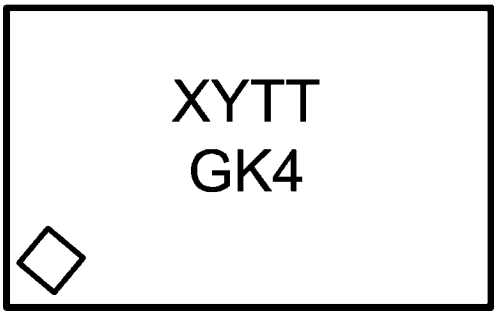
LM48556TL Marking



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Top View
XY = Date Code
TT = Lot Traceability
G = Boomer Family
K4 = LM48556TL

TABLE 1. Bump Descriptions

Bump	Name	Description
A1	OUT-	Amplifier Inverting Output
A2	SV_{DD}	Signal Power Supply - Positive
A3	IN+	Amplifier Non-inverting Input
B1	SV_{SS}	Signal Power Supply - Negative
B2	OUT+	Amplifier Non-inverting Output
B3	IN-	Amplifier Inverting Input
C1	CPV_{SS}	Charge Pump Output Voltage
C2	C1P	Charge Pump Flying Capacitor Positive Terminal
C3	$\overline{SD}$	Active Low Reset Input. Connect to V_{DD} for normal operation. Drive $\overline{SD}$ low to disable.
D1	C1N	Charge Pump Flying Capacitor Negative Terminal
D2	PGND	Power Ground
D3	PV_{DD}	Power Supply

Ordering Information

Order Number	Package	Package Dwg #	Transport Media	MSL	Green Status	Features
LM48556TL	12 bump micro SMD	TLA121AA	250 units on tape and reel	1	RoHS and no Sb/Br	
LM48556TLX	12 bump micro SMD	TLA121AA	3000 units on tape and reel	1	RoHS and no Sb/Br	

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (SV_{DD}, PV_{DD}) (Note 1)	4.8V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Rating(Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (TL)	114°C/W
Soldering Information	
See AN-1112 Micro SMD Wafer Level Chip Scale	

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (SV_{DD}, PV_{DD})	$2.7V \le \_V_{DD} \le 4.5V$

Electrical Characteristics V_{DD} = 3.6V (Note 2)

The following specifications apply for V_{DD} = 3.6V, $A_{V\text{-}BTL}$ = 20dB (R_F = 200kΩ, R_{IN} = 20kΩ), Z_L = 15Ω+1µF, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48556		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V	4.8	7	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{SD}}$ = GND (Note 8)	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	C_{IN} = 0.47µF, A_V = 1V/V (0dB)	0.6	4	mV (max)
T_{WU}	Wake-up Time		0.5		ms
V_{OUT}	Output Voltage Swing	THD+N = 1% (max); f = 1kHz	14.2		V_{PP}
		THD+N = 1% (max); f = 10kHz	11.5	11	V_{PP} (min)
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 11V_{PP}, f = 1kHz			
		A_V = 0dB	0.005		%
		A_V = 20dB	0.03		%
ε_{OS}	Output Noise	A-weighted filter, V_{IN} = 0V Input referred	8		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, f = 217Hz	80	60	dB (min)
CMRR	Common Mode Rejection Ratio	Input Referred	70	60	dB (min)
V_{LH}	Logic High Threshold Voltage			1.2	V (min)
V_{LL}	Logic Low Threshold Voltage			0.45	V (max)

Electrical Characteristics V_{DD} = 4.5V (Note 2)

The following specifications apply for V_{DD} = 4.5V, $A_{V\text{-}BTL}$ = 20dB (R_F = 200kΩ, R_{IN} = 20kΩ), Z_L = 15Ω+1µF, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48556		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V	6.5	10	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{SD}}$ = GND (Note 8)	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	C_{IN} = 0.47µF, A_V = 1V/V (0dB)	0.6	4	mV (max)
T_{WU}	Wake-up Time		0.5		ms (max)
V_{OUT}	Output Voltage Swing	THD+N = 1% (max); f = 1kHz	17.5		V_{PP}
		THD+N = 1% (max); f = 10kHz	14.6	14	V_{PP} (min)
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 14V_{PP}, f = 1kHz			
		A_V = 0dB	0.005		%
		A_V = 20dB	0.03		%
ε_{OS}	Output Noise	A-weighted filter, V_{IN} = 0V Input referred	8		µV

Symbol	Parameter	Conditions	LM48556		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, f = 217Hz,	80	60	dB (min)
CMRR	Common Mode Rejection Ratio	Input Referred	70	60	dB (min)
V_{LH}	Logic High Threshold Voltage			1.2	V (min)
V_{LL}	Logic Low Threshold Voltage			0.45	V (max)

Note 1: *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

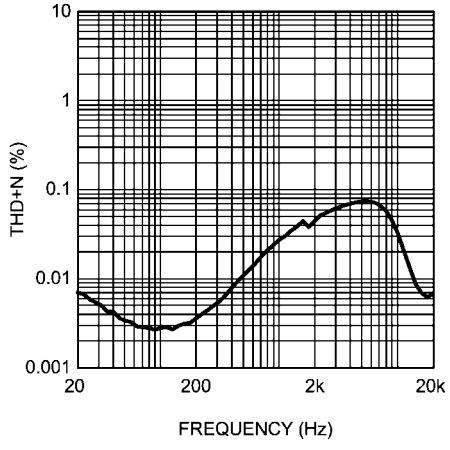
Note 6: Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 8: Shutdown current is measured in a normal room environment. The $\overline{SD}$ pin should be driven as close as possible to GND for minimum shutdown current.

Typical Performance Characteristics
(Z_L = 15Ω+1µF, A_V = 20dB, BW = 22kHz)

THD+N vs Frequency
V_{DD} = 2.7V, V_O = 8V_{PP}



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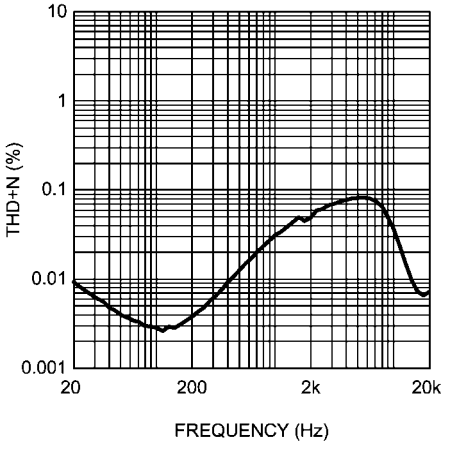
THD+N vs Frequency
V_{DD} = 3.6V, V_O = 14.2V_{PP}



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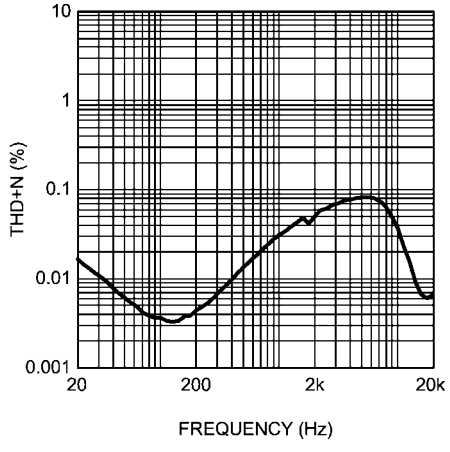
THD+N vs Frequency
V_{DD} = 4.5V, V_O = 17.5V_{PP}



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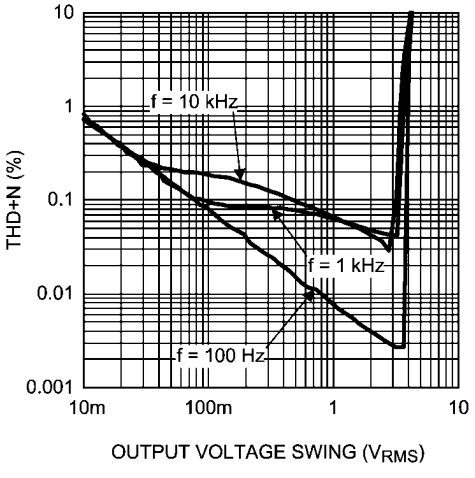
THD+N vs Output Voltage Swing
V_{DD} = 2.7V, f = 1kHz



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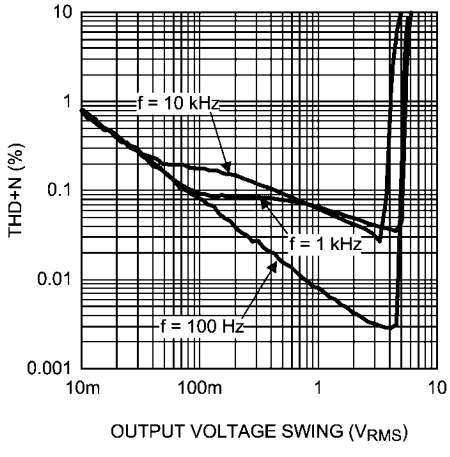
THD+N vs Output Voltage Swing
V_{DD} = 3.6V, f = 1kHz



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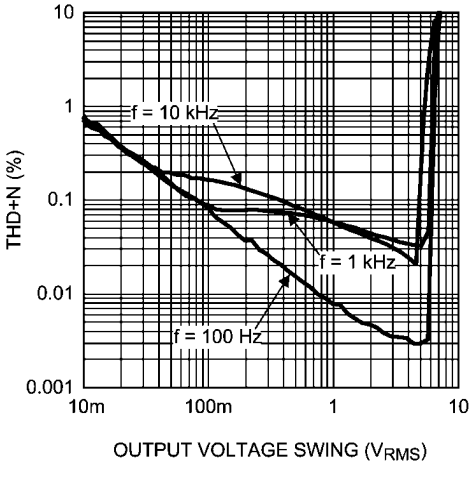
THD+N vs Output Voltage Swing
V_{DD} = 4.5V, f = 1kHz



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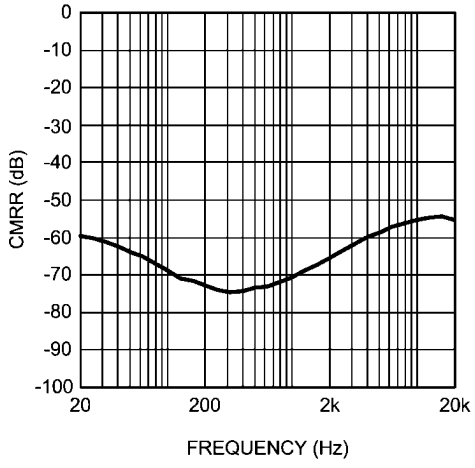
CMRR vs Frequency
V_{DD} = 2.7V, Input referred



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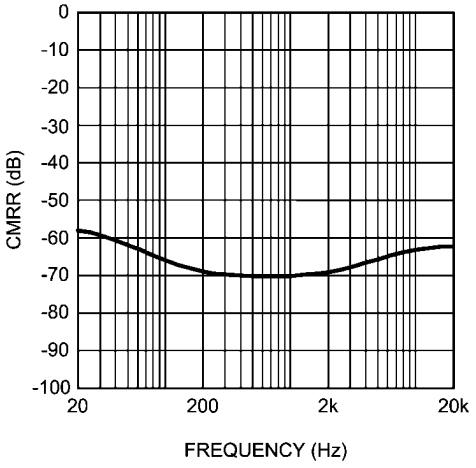
CMRR vs Frequency
V_{DD} = 3.6V, Input referred



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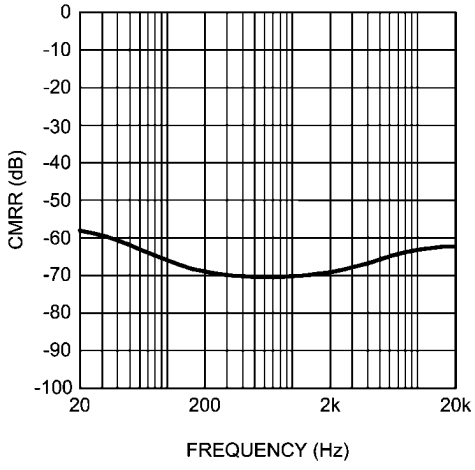
CMRR vs Frequency
V_{DD} = 4.5V, Input referred



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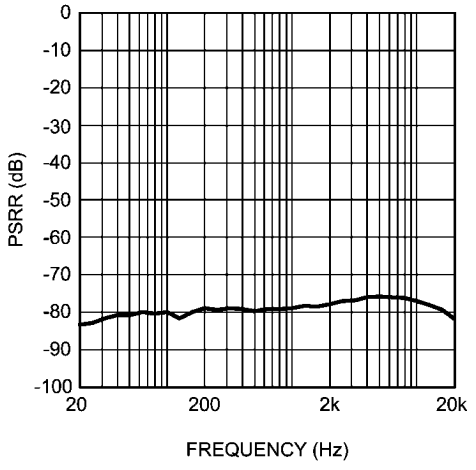
PSRR vs Frequency
V_{DD} = 2.7V, Input referred



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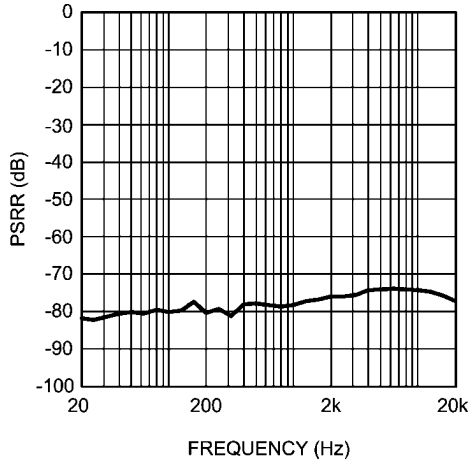
PSRR vs Frequency
V_{DD} = 3.6V, Input referred



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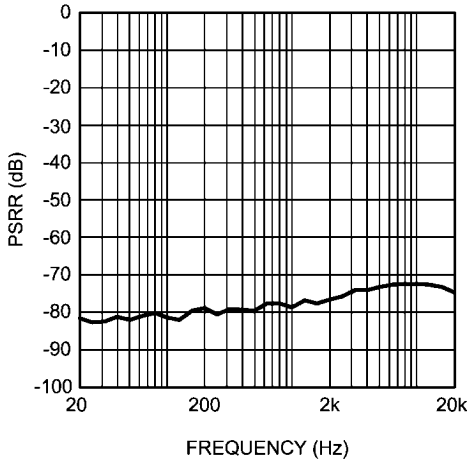
PSRR vs Frequency
V_{DD} = 4.5V, Input referred



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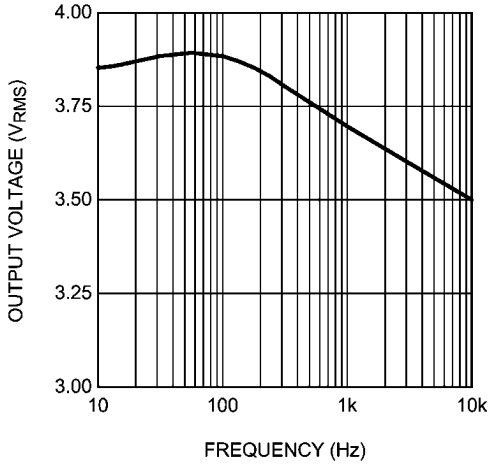
Output Voltage vs Frequency
V_{DD} = 2.7V, THD+N = 1%



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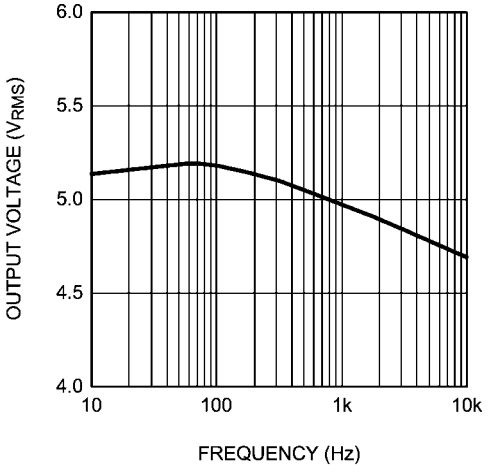
Output Voltage vs Frequency
V_{DD} = 3.6V, THD+N = 1%



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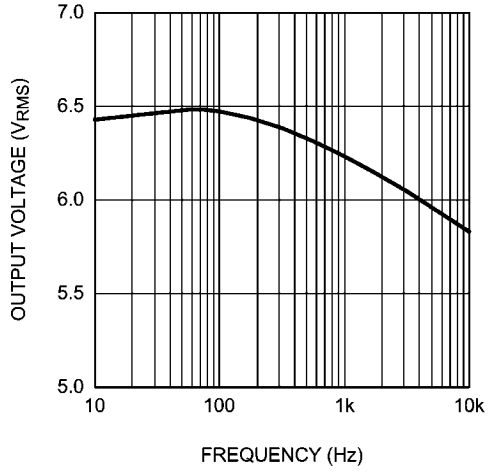
Output Voltage vs Frequency
V_{DD} = 4.5V, THD+N = 1%



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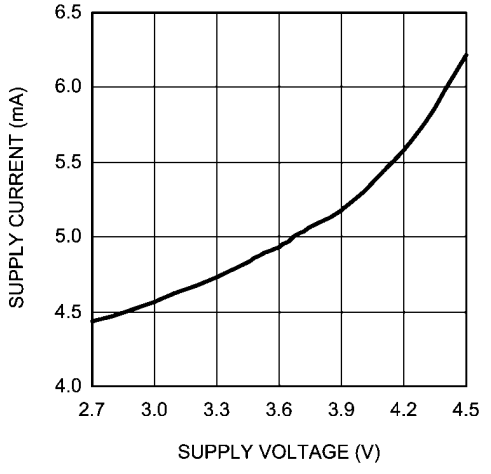
Supply Current vs Supply Voltage
V_{IN} = GND, No Load



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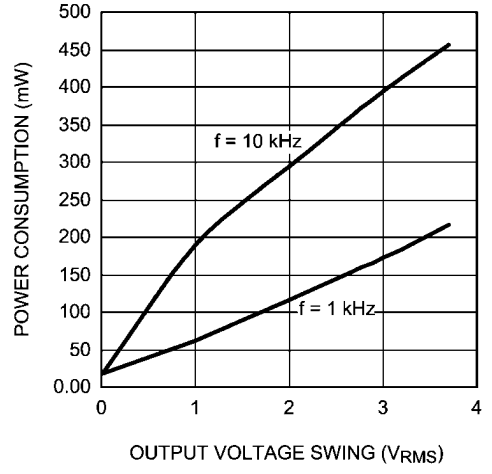
Power Consumption vs Output Voltage Swing
V_{DD} = 2.7V, THD+N ≤ 1%



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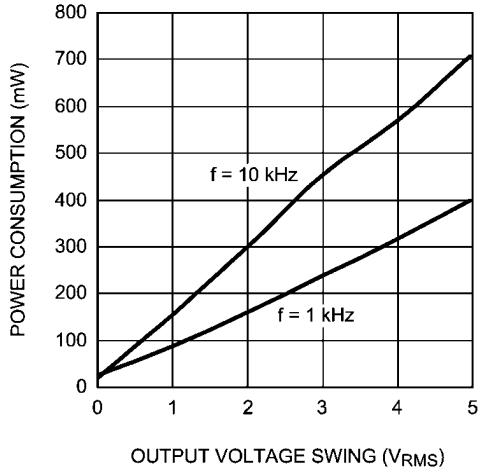
Power Consumption vs Output Voltage Swing
V_{DD} = 3.6V, THD+N ≤ 1%



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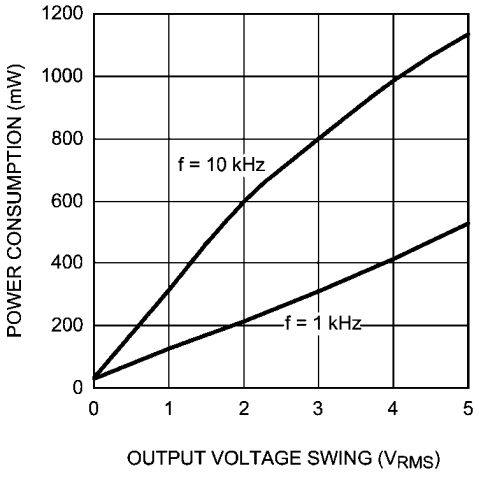
Power Consumption vs Output Voltage Swing
V_{DD} = 4.5V, THD+N ≤ 1%



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Application Information

GENERAL AMPLIFIER FUNCTION

The LM48556 is a fully differential ceramic speaker driver that utilizes National's inverting charge pump technology to deliver the high drive voltages required by ceramic speakers, without the need for noisy, board-space consuming inductive based regulators. The low-noise, inverting charge pump creates a negative supply (CPV_{SS}) from the positive supply (PV_{DD}). Because the amplifiers operate from these bipolar supplies, the maximum output voltage swing for each amplifier is doubled compared to a traditional single supply device. Additionally, the LM48556 is configured as a bridge-tied load (BTL) device, quadrupling the maximum theoretical output voltage range when compared to a single supply, single-ended output amplifier, see *Bridged Configuration Explained* section. The charge pump and BTL configuration allow the LM48556 to deliver over $17V_{P-P}$ at 1kHz to a 1µF ceramic speaker while operating from a single 4.5V supply .

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM48556 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM48556 can be used without input coupling capacitors when configured with a differential input signal.

BRIDGE CONFIGURATION EXPLAINED

The LM48556 is designed to drive a load differentially, a configuration commonly referred to as a bridge-tied load (BTL). The BTL configuration differs from the single-ended configuration, where one side of the load is connected to ground. A BTL amplifier offers advantages over a single-ended device. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Any component common to both outputs is cancelled, thus there is no net DC voltage across the load, eliminating the DC blocking capacitors required by single-ended, single-supply amplifiers.

SHUTDOWN FUNCTION

The LM48556 features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and reduce supply current to 0.1µA. Switch $\overline{SD}$ between V_{DD} and GND for minimum current consumption in shutdown. The LM48556 may be disabled with shutdown voltages less than 0.45V, however, the idle current will be greater than the typical 0.1µA value.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 4.7µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C_{SS} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (C_{SS})

The value and ESR of the hold capacitor (C_{SS}) directly affects the ripple on CPV_{SS}. Increasing the value of C_{SS} reduces output ripple. Decreasing the ESR of C_{SS} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Gain Setting Resistor Selection

The amplifier gain of the LM48556 is set by four external resistors, two per each input, $R_{IN\_}$ and $R_{F\_}$ (Figure 1). The amplifier gain is given by equation (1):

$$A_V = R_F / R_{IN} \quad (V/V) \qquad (1)$$

Careful matching of the resistor pairs, R_{F+} and R_{F-}, and R_{IN+} and R_{IN-}, is required for optimum performance. Any mismatch between the resistors results in a differential gain error that leads to an increase in THD+N, decrease in PSRR and CMRR, as well as an increase in output offset voltage. Resistors with a tolerance of 1% or better are recommended.

The gain setting resistors should be placed as close to the device as possible. Keeping the input traces close together and of the same length increases noise rejection in noisy environments. Noise coupled onto the input traces which are physically close to each other will be common mode and easily rejected.

Feedback Capacitor Selection

Due to their capacitive nature, ceramic speakers poorly reproduce high frequency audio content. At high frequencies, a ceramic speaker presents a low impedance load to the amplifier, increasing the required drive current. The higher output current can drive the device into clipping, increasing THD+N. Low-pass filtering the audio signal improves audio quality by decreasing the signal amplitude at high frequencies, reducing the speaker drive current. Adding a capacitor in parallel with each feedback resistor creates a simple low-pass filter with the -3dB point determined by equation (2):

$$f_{-3dB} = 1 / 2\pi R_F C_F \quad (Hz) \qquad (2)$$

Where R_F is the value of the feedback resistor determined by equation (1) in the *Gain Setting Resistors Selection* section, and C_F is the value of the feedback capacitor. The feedback capacitor is optional and not required for normal operation.

Input Capacitor Selection

Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48556. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation (3) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (Hz) \qquad (3)$$

Where the value of R_{IN} is determined by equation (1) in the *Gain Setting Resistor Selection* section.

When the LM48556 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 1% or better are recommended for impedance matching and improved CMRR and PSRR.

SINGLE-ENDED AUDIO AMPLIFIER CONFIGURATION

The LM48556 is compatible with single-ended sources. Figure 2 shows the typical single-ended applications circuit. In

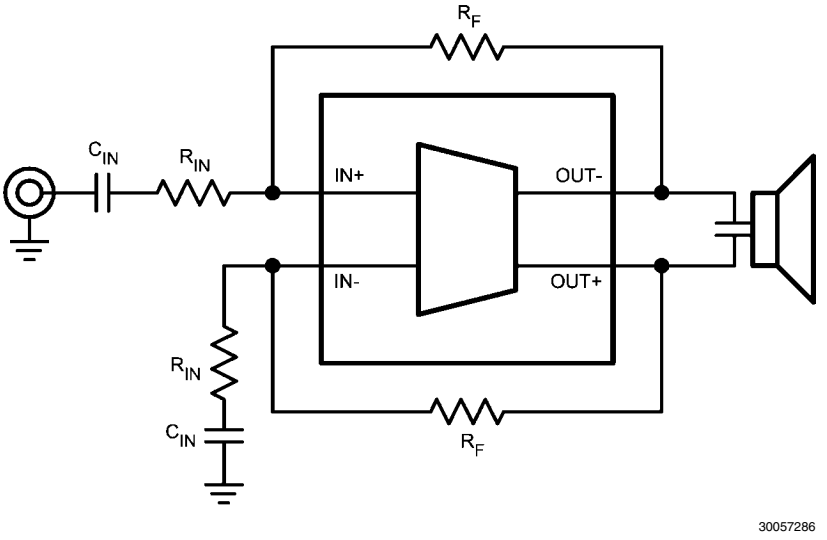

FIGURE 2. Single-Ended Input Configuration

Bill Of Materials

Component	Description	Designator	Footprint	Quantity
LM48556TL	LM48556TL	LM48556TL	LM48556TL	1
Capacitor	4.7µF, ceramic, low ESR (<0.1Ω) 16V, -40°C to +85°C	C1	CR3216-1206	1
Capacitor	82µF, 16V, -40°C to +85°C	C_{F+}	CR2012-0805	1
Capacitor	82µF, 16V, -40°C to +85°C	C_{F-}	CR2012-0805	1
Capacitor	0.47µF, 16V, -40°C to +85°	C_{IN+}	CR2012-0805	1
Capacitor	0.47µF, 16V, -40°C to +85°C	C_{IN-}	CR2012-0805	1
Capacitor	4.7µF, 16V, -40°C to +85°C	C_{S1}	CR3216-1206	1
Capacitor	0.1µF ceramic, 16V, -40°C to +85°C	C_{S2}	CR2012-0805	1
Capacitor	10µF ceramic, low ESR (<0.1Ω) 16V, -40°C to +85°C	C_{SS}	CR3216-1206	1
Header, 2–Pin	Header 2	IN	HDR1X2	1
Resistor	200kΩ	R_{F+}	CR2012-0805	1
Resistor	200kΩ	R_{F+}	CR2012-0805	1
Resistor	200kΩ	R_{IN+}	CR2012-0805	1
Resistor	200kΩ	R_{IN-}	CR2012-0805	1
Header, 2–Pin	Header 2	SPEAKER	HDR1X2	1
Header, 2–Pin	Header 2	V_{DD}	HDR1X2	1
Header, 3–Pin	3–pole jumper	J1	3–pole jumper	1

Demonstration Board Schematic

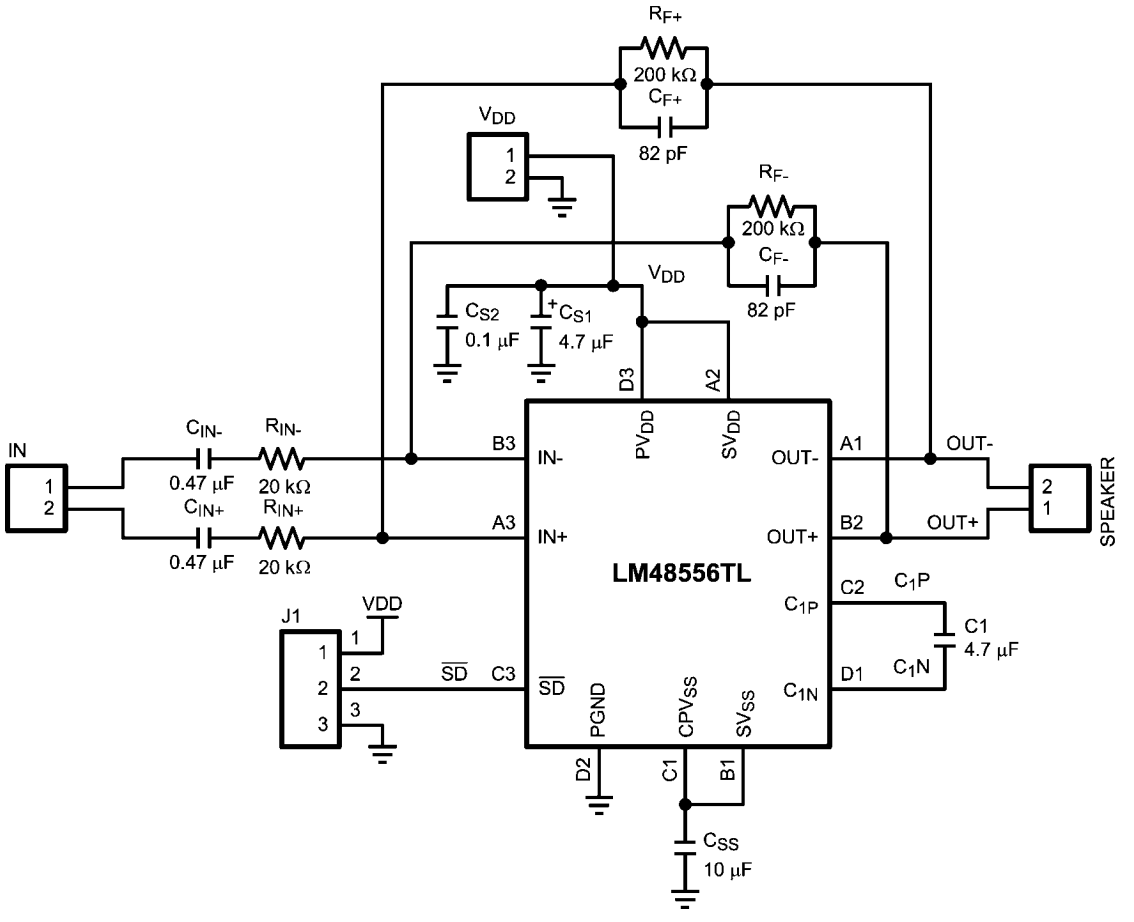

FIGURE 3: Demo Board Schematic

Demonstration Board PCB Views

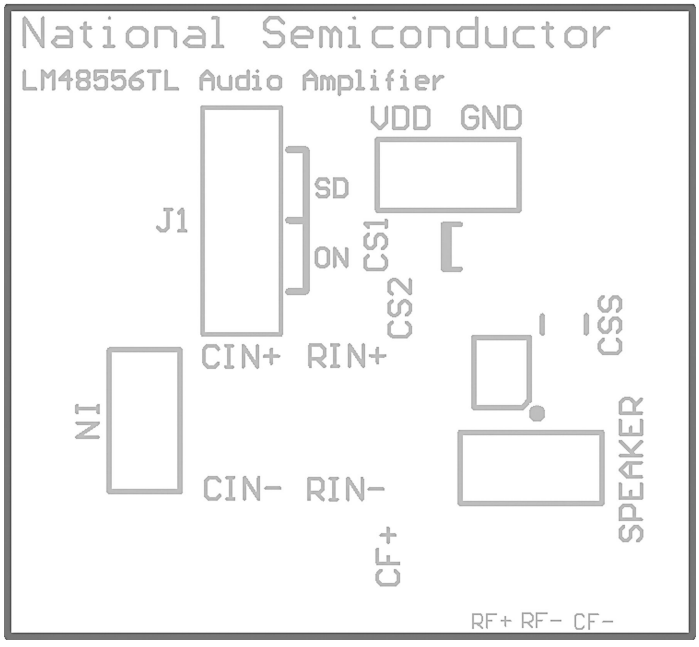

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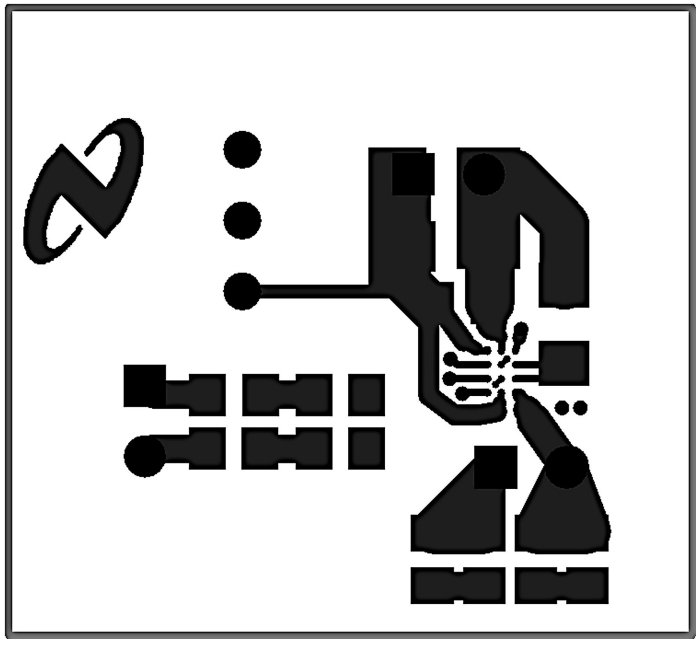
FIGURE 4: Top Overlay



300572b5

FIGURE 5: Top Layer

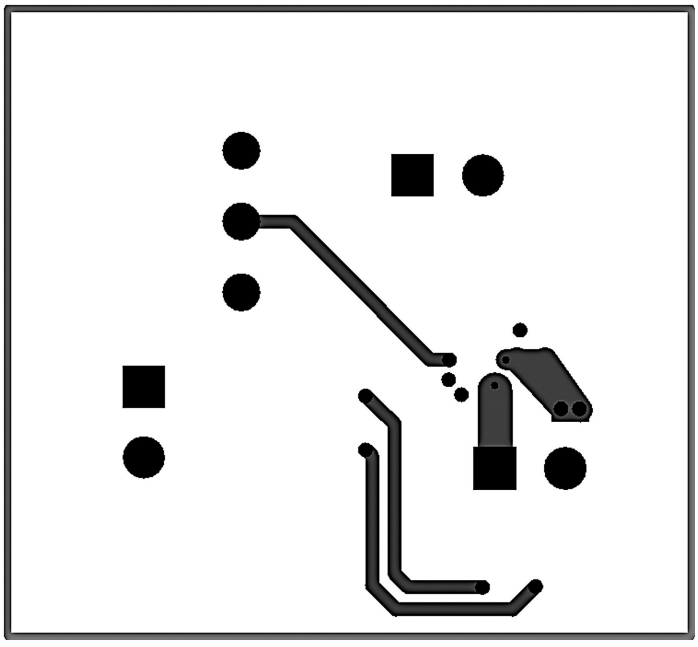


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FIGURE 6: Mid Layer 1

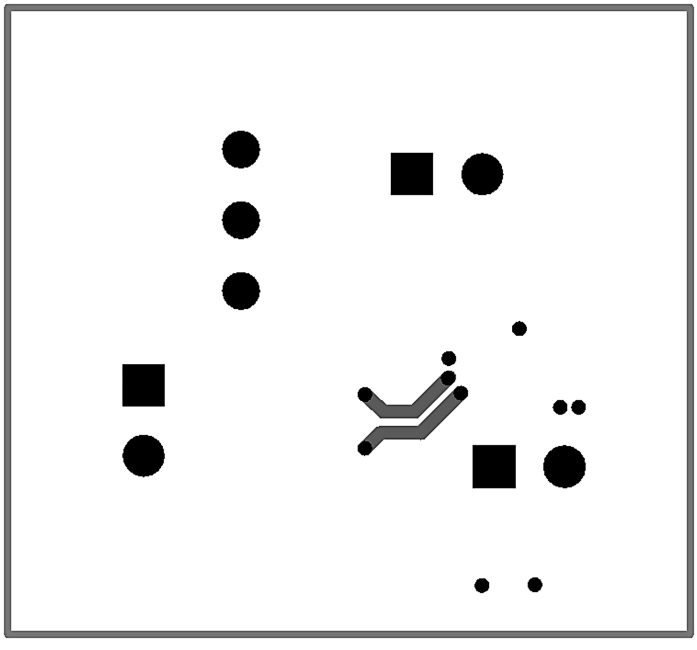

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FIGURE 7: Mid Layer 2

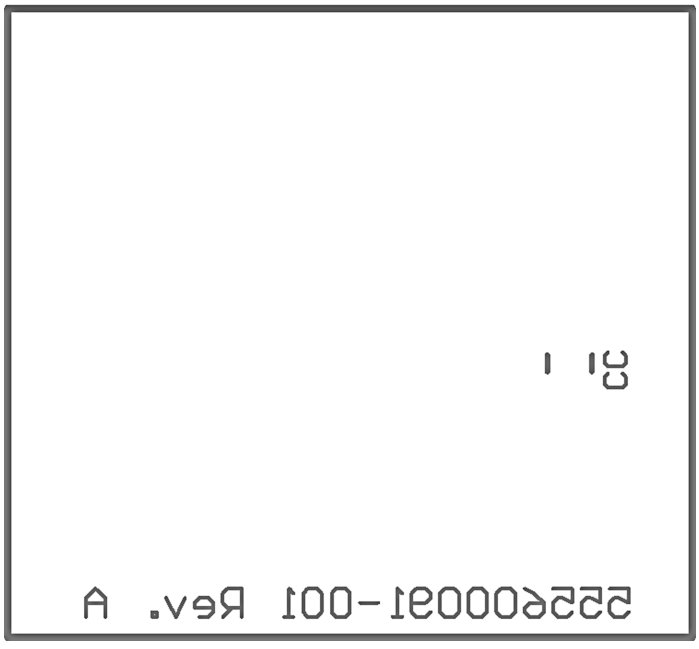

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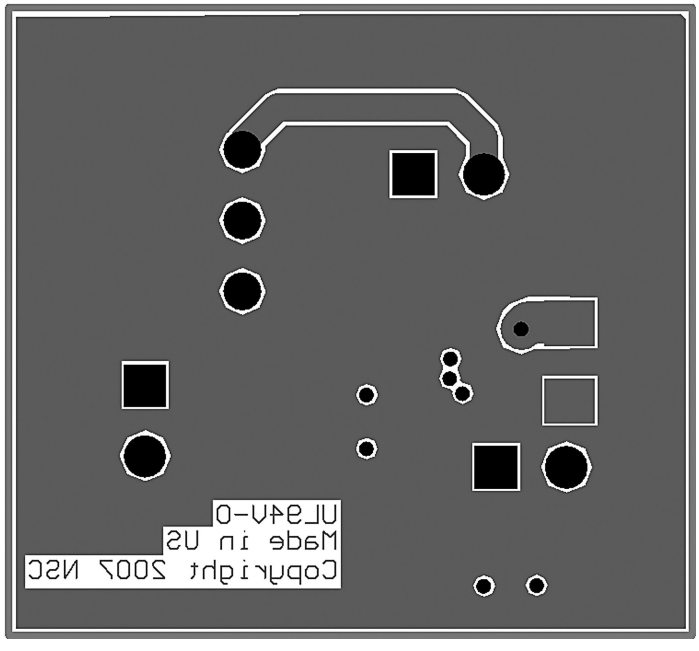
FIGURE 8: Bottom Overlay



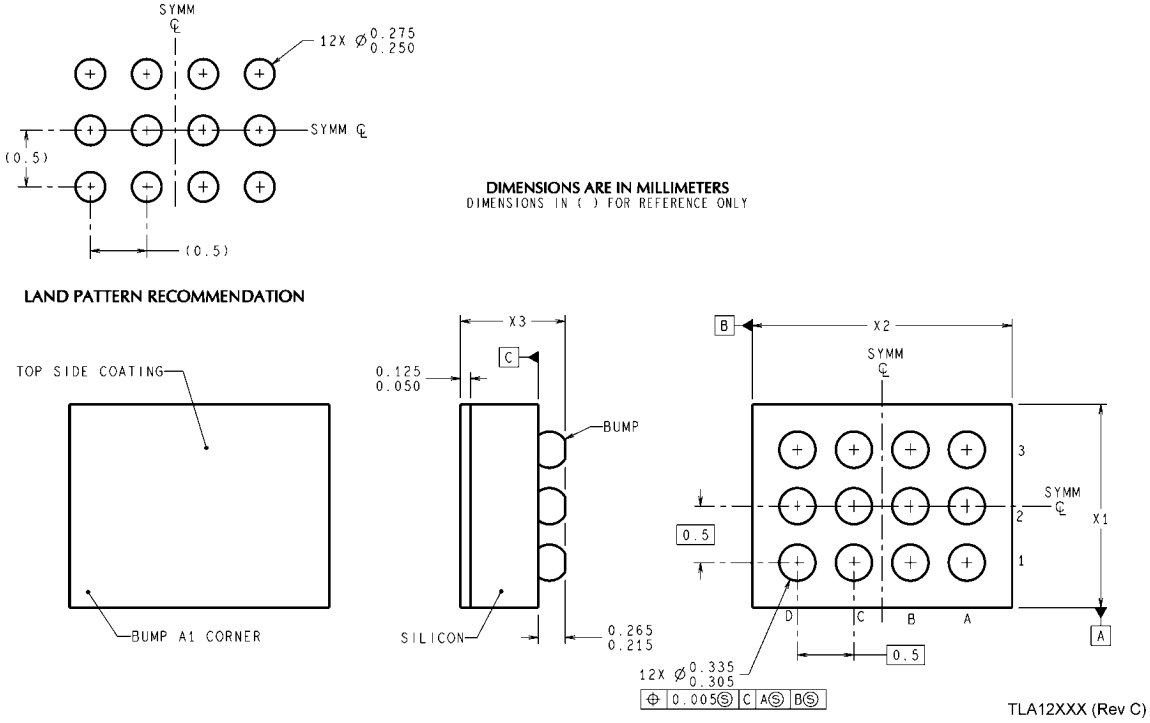
300572b1

FIGURE 9: Bottom Layer

Revision History

Rev	Date	Description
1.0	06/03/08	Initial release.

Physical Dimensions inches (millimeters) unless otherwise noted



12 Bump micro SMD
Order Number LM48556TL, LM48556TLX
NS Package Number TLA121AA
X_1 = 1488µm, X_2 = 1996µm, X_3 = 600µm

Notes

Notes

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